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FISH & RICHARDSON, PC
P.O. BOX 1022
MINNEAPOLIS, MN 55440-1022

EXAMINER	
LI, AIMEE J	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/760,509	WOLRICH ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2006 and 22 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,15-26 and 30-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,15-26 and 30-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/22/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-7, 15-26, and 30-34 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received 08 December 2006; One-Month Extension of Time as received 08 December 2006; and IDS as received 22 February 2007.

Information Disclosure Statement

3. The information disclosure statement filed 22 February 2007 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because reference EO (Paver, et al., "Register Locking in an Asynchronous Microprocessor") in the IDS was previously considered in the IDS filed 03 January 2005 and reference 49 in the third eIDS (Parady, U.S. Patent Number 5,933,627) was cited in a PTO-892 mailed 09 March 2004. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

Claim Rejections – 35 USC §103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5 and 15-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent Number 5,933,627 (herein referred to as Parady) in view of Dreibelbis et al., U.S. Patent Number 5,875,470 (herein referred to as Dreibelbis).

6. Regarding claims 1 and 15, taking claim 1 as exemplary, Parady has taught an execution unit for execution of multiple context threads comprises:

a. An arithmetic logic unit to process data for executing threads (Parady Col.2 lines 18-29 and Col.3 lines 19-25),

b. Control logic to control the operation of the arithmetic logic unit (Parady Col.3 lines 10-18),

c. A general purpose register set to store and obtain operands for the arithmetic logic unit, the register set comprising a plurality of two-ported random access memory devices assembled into banks (Parady 48 of Fig.1/Fig.3), each bank being capable of performing a read and a write to two different words with two ports in the same processor cycle (Parady Fig.3 and Col.3 lines 43-49). Here, because the register file contains ten ports (Parady 48 of Fig.1) and four banks (Parady Col.3 lines 43-49), there are inherently at least two ports per bank, therefore allowing each bank to write or read at least one word per bank per cycle.

7. Parady has not explicitly taught the register set comprising two effective read ports and one effective write port, wherein the arithmetic logic unit can write to each bank in the general purpose register set using the one effective write port. However, Parady has taught that register files often have multiple ports (Parady column 5, lines 30-31). Dreibelbis has taught the register

set comprising two effective read ports and one effective write port, wherein the arithmetic logic unit can write to each bank in the general purpose register set using the one effective write port (Dreibelbis Abstract; column 2, lines 6-29; column 3, lines 11-19 and 50-62; column 4, lines 18-31; column 4, line 46 to column 5, line 24; column 5, lines 39-55; Figure 1A; Figure 1B). Dreibelbis has taught that their banking system is usable in a system with several processes (Dreibelbis column 8, lines 16-40), such as the multiple threaded system in Parady. A person of ordinary skill in the art at the time the invention was made, and as taught by Dreibelbis, would have recognized that the memory bank system of Dreibelbis provides extraordinarily high parallelism and significantly improves slower processor access to a shared cache (Dreibelbis column 3, lines 11-19 and 50-55). Therefore, it would have been to a person of ordinary skill in the art at the time the invention was made to incorporate the memory banking of Dreibelbis in the device of Parady to increase parallelism and improve cache access speed.

8. Claim 15 is nearly identical to claim 1, differing in its parent claim, but encompassing the same scope. Therefore, claim 15 is rejected for the same reasons as claim 1.

9. Regarding claims 2 and 16, taking claim 2 as exemplary, Parady in view of Dreibelbis has taught the execution unit of claim 1, wherein the register set is logically partitioned into a plurality of relatively addressable windows (Parady Col.3 lines 43-49 and Col.4 lines 1-8). Here, the register file is divided into four register files for four threads (Parady Col.3 lines 43-45), and there is a thread field in each instruction that identifies which thread an instructions operands come from (Parady Col.4 lines 1-8). This makes each register in each register file relatively addressable, being differentiated from each other relative to their 2-bit thread field.

10. Claim 16 is nearly identical to claim 2, differing in its parent claim, but encompassing the same scope. Therefore, claim 16 is rejected for the same reasons as claim 2.

11. Regarding claims 3 and 17, taking claim 3 as exemplary, Parady in view of Dreibelbis has taught the execution unit of claim 2, wherein the number of windows of the register set is related to the number of threads that can execute in the processor (Parady Col.3 lines 43-49).

12. Claim 17 is nearly identical to claim 3, differing in its parent claim, but encompassing the same scope. Therefore, claim 17 is rejected for the same reasons as claim 3.

13. Regarding claims 4, 18 and 21, taking claim 4 as exemplary, Parady in view of Dreibelbis has taught the execution unit of claim 1, wherein relative addressing allows an executing thread to access the register set relative to the starting point of a window (Parady Col.3 lines 43-49 and Col.4 lines 1-8). Here, the register file is divided into four register files for four threads (Parady Col.3 lines 43-45), and there is a thread field in each instruction that identifies which thread an instructions operands come from (Parady Col.4 lines 1-8). This makes each register in each register file relatively addressable, being differentiated from each other relative to their 2-bit thread field, allowing a thread to access registers associated with its 2-bti thread field.

14. Claims 18 and 21 are nearly identical to claim 4, differing in their parent claims, but encompassing the same scope. Therefore, claim 18 and 21 are rejected for the same reasons as claim 4.

15. Regarding claims 5 and 22, taking claim 5 as exemplary, Parady in view of Dreibelbis has taught the execution unit of claim 1, wherein the register set is absolutely addressable, where the register set may be accessed for an executing thread by providing and exact address (Parady Col.3 lines 43-49 and Col.4 lines 1-8, 18-22). As shown above in paragraphs 23 and 27, the

register set is relatively addressable using a 2-bit thread field that specifies which thread, and consequently which register window, an instruction's operands come from. However, the 2-bit thread field can also be used to inter-relate two threads (Parady Col.4 lines 18-22), thus allowing one thread to access to any other register in any other thread, providing absolute addressability.

16. Claim 22 is nearly identical to claim 5, differing in its parent claim, but encompassing the same scope. Therefore, claim 22 is rejected for the same reasons as claim 5.

17. Regarding claim 19, Parady has taught a processor unit comprising:

a. An execution unit for execution of multiple context threads, the execution unit comprising:

i. An arithmetic logic unit to process data for executing threads (Parady Col.2 lines 18-29 and Col.3 lines 19-25),

ii. Control logic to control the operation of the arithmetic logic unit (Parady Col.3 lines 10-18);

iii. A general purpose register set (Parady 48 of Fig.1/Fig.3) to store and obtain operands for the arithmetic logic unit (Parady see Fig.3), the register set comprising a plurality of two-ported random access memory devices. While not taught explicitly, it is inherent in the operation of a register file that it has at least one port to read and one port to write data in and out of the register file, and thus inherently a register file has at least two ports.

18. Parady has not explicitly taught the register set comprising two effective read ports and one effective write port; and a data link between the arithmetic logic unit and the one effective

write port of the general purpose register set, wherein the data link allows the arithmetic logic unit to write to different two-ported random access memory devices in the general purpose register set through the one effective write port. However, Parady has taught that register files often have multiple ports (Parady column 5, lines 30-31). Dreibelbis has taught the register set comprising two effective read ports and one effective write port; and a data link between the arithmetic logic unit and the one effective write port of the general purpose register set, wherein the data link allows the arithmetic logic unit to write to different two-ported random access memory devices in the general purpose register set through the one effective write port (Dreibelbis Abstract; column 2, lines 6-29; column 3, lines 11-19 and 50-62; column 4, lines 18-31; column 4, line 46 to column 5, line 24; column 5, lines 39-55; Figure 1A; Figure 1B). Dreibelbis has taught that their banking system is usable in a system with several processes (Dreibelbis column 8, lines 16-40), such as the multiple threaded system in Parady. A person of ordinary skill in the art at the time the invention was made, and as taught by Dreibelbis, would have recognized that the memory bank system of Dreibelbis provides extraordinarily high parallelism and significantly improves slower processor access to a shared cache (Dreibelbis column 3, lines 11-19 and 50-55). Therefore, it would have been to a person of ordinary skill in the art at the time the invention was made to incorporate the memory banking of Dreibelbis in the device of Parady to increase parallelism and improve cache access speed.

19. Regarding claim 20, Parady in view of Dreibelbis has taught the processor of claim 19, wherein the register set is logically partitioned into a plurality of relatively addressable windows, where the number of windows of the register set is related to the number of threads that can execute in the processor (Parady Col.3 lines 43-49 and Col.4 lines 1-8). Here, the register file is

divided into four register files for four threads (Parady Col.3 lines 43-45), and there is a thread field in each instruction that identifies which thread an instructions operands come from (Parady Col.4 lines 1-8). This makes each register in each register file relatively addressable, being differentiated from each other relative to their 2-bit thread field.

20. Regarding to claims 30-32, Parady in view of Dreibelbis has taught

a. Wherein the register set comprises a first number *n* of two-ported random access memory devices, a second number *r* of effective read ports, and a third number *w* of effective write ports, where $n \geq 2$, $2 \leq r \leq n$, and $2 \leq w \leq n-1$ (Applicant's claim 30) (Dreibelbis Abstract; column 2, lines 6-29; column 3, lines 11-19 and 50-62; column 4, lines 18-31; column 4, line 46 to column 5, line 24; column 5, lines 39-55; Figure 1A; Figure 1B);

b. Wherein storing and obtaining operands comprises storing and obtaining operands within the general purpose register comprising a first number *n* of two-ported random access memory devices, a second number *r* of effective read ports, and a third number *w* of effective write ports, where $n \geq 2$, $2 \leq r \leq n$, and $2 \leq w \leq n-1$ (Applicant's claim 31) (Dreibelbis Abstract; column 2, lines 6-29; column 3, lines 11-19 and 50-62; column 4, lines 18-31; column 4, line 46 to column 5, line 24; column 5, lines 39-55; Figure 1A; Figure 1B); and

c. Wherein the general purpose register set comprises a first number *n* of two-ported random access memory devices, a second number *r* of effective read ports, and a third number *w* of effective write ports, where $n \geq 2$, $2 \leq r \leq n$, and $2 \leq w \leq n-1$ (Applicant's claim 32) (Dreibelbis Abstract; column 2, lines 6-29; column 3, lines

11-19 and 50-62; column 4, lines 18-31; column 4, line 46 to column 5, line 24; column 5, lines 39-55; Figure 1A; Figure 1B).

21. Referring to claims 33-34, Parady in view of Dreibelbis has taught

a. Wherein memory addresses of the banks are interleaved (Applicants' claim 33) (Dreibelbis Abstract; column 2, lines 6-29; column 3, lines 11-19 and 50-62; column 4, lines 18-31; column 4, line 46 to column 5, line 24; column 5, lines 39-55; Figure 1A; Figure 1B); and

b. Wherein memory addresses of the banks are interleaved (Applicants' claim 34) (Dreibelbis Abstract; column 2, lines 6-29; column 3, lines 11-19 and 50-62; column 4, lines 18-31; column 4, line 46 to column 5, line 24; column 5, lines 39-55; Figure 1A; Figure 1B).

22. Claims 6-7 and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parady, U.S. Patent Number 5,933,627 (herein referred to as Parady) in view of Dreibelbis et al., U.S. Patent Number 5,875,470 (herein referred to as Dreibelbis), as applied to claims 1-5 above, and further in view of Waldspurger et al., "*Register Relocation: Flexible Contexts for Multithreading*" (herein referred to as Waldspurger).

23. Regarding claims 6 and 23, taking claim 6 as exemplary, Parady has taught the execution unit of claim 1, wherein the control logic further comprises:

a. Context switching logic (Parady 112 of Fig.3) fed by signals from a plurality of shared resources (Parady Col.3 lines 57-65).

24. Parady has not explicitly taught wherein the signals cause the context event logic to indicate that threads are either available or unavailable for execution.

25. However, Waldspurger has taught a context switch scheduler that comprises a circularly-linked "ready queue" which determines which contexts are ready for execution when a context switch is required in order to provide fast context switching (Waldspurger paragraph 1 of Sec. 2.2). One of ordinary skill in the art would have recognized that it is a primary goal of microprocessor designers to reduce delays in their datapath, such as those introduced when a context switch is required, thereby increasing the speed and throughput of their processors. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady to provide threads that are available for execution in the manner of Waldspurger so that context switches can be performed fast, thus increasing the processor speed.

26. Regarding claims 7 and 23, taking claim 7 as exemplary, Parady in view of Waldspurger has taught the execution unit of claim 6, wherein the control logic addresses a set of memory locations for storing a list of available threads that correspond to threads that are ready to be executed and a set of memory locations for storing a list of unavailable threads that are not ready to be executed (see above paragraph 27 and Waldspurger paragraph 1 of Sec. 2.2). Here, the "set of memory locations" is a circularly-linked queue, such that the next threads that are ready to be executed are at the "head" of the list, while those that are not ready, or were recently switched from, reside at the "tail" of the list (Waldspurger Sec. 2.2).

27. Claim 23 is nearly identical to claims 6 and 7, differing in its parent claim, but encompassing the same scope as claims 6 and 7. Therefore, claim 23 is rejected for the same reasons as claims 6 and 7.

28. Regarding claim 24, Parady in view of Waldspurger has taught the execution unit of claim 23, wherein execution of a context swap instruction causes a currently running thread to be

swapped out to the unavailable thread memory set and a thread from the available thread memory set to begin execution within a single execution cycle (Parady Fig.3, Col.2 lines 18-25, Col.3 lines 57-65 and Waldspurger paragraphs 2-5 of Sec. 2.2.). Here, a load or store operation signals a context switch (Parady Fig.3 and Col.3 lines 57-65), and the context switch steps store the current context at the "tail" of the circularly-linked list and update the current context to be the thread that was next in line to be executed (Waldspurger paragraphs 2-5 of Sec. 2.2).

29. Regarding claim 25, Parady in view of Waldspurger has taught the execution unit of claim 23, wherein execution of the context swap instruction specifies one of the signal inputs and upon receipt of the specified signal input causes the swapped out thread to be stored in the available thread memory set (Parady Fig.3, Col.2 lines 18-25, Col.3 lines 57-65 and Waldspurger paragraphs 2-5 of Sec. 2.2.). Here, a load or store operation signals a context switch (Parady 114 of Fig.3 and Col.3 lines 57-65), and the context switch steps store the current context at the "tail" of the circularly-linked list and update the current context to be the thread that was next in line to be executed (Waldspurger paragraphs 2-5 of Sec. 2.2).

30. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parady in view of Dreibelbis in view of Waldspurger, as applied to claim 23 above, and further in view of Trauben et al., U.S. Patent No. 5,509,130.

31. Regarding claim 26, Parady in view of Waldspurger has taught the execution unit of claim 23, but have not explicitly taught wherein execution of the context swap instruction specifies a defer one operation which causes execution of one more instruction and then causes the current context to be swapped out.

32. However, Trauben has taught a branch delay instruction which causes the execution of one instruction before changing context in order to hide the latency of computing and fetching the branch target (Trauben Col.14 lines 41-60). One of ordinary skill in the art would have recognized that it is desirable to reduce the amount of delay in a microprocessor and thus allow faster execution times. Therefore, one of ordinary skill in the art would have found it obvious to modify the processor of Parady in view of Waldspurger to include a branch delay instruction which allows an instruction to execute while computing and fetching a branch target so that the latency of the operation can be avoided.

Response to Arguments

33. Applicant's arguments filed 08 December 2006 have been fully considered but they are not persuasive. Applicant's argue in essence on pages 9-16

> ...Parady and Dreibelbis neither describe nor suggest a register set that comprises a plurality of two-ported random access memory devices and two effective read ports and one effective write port...

34. This has not been found persuasive. Parady has taught in Figure 1, element 48 an integer register file with 10 ports (7 read and 3 write) and element 50 a floating-point register file with 8 ports (5 read and 3 write). This means that the register files have at least two-ports and it meets the requirements of "a plurality of two-ported random access memory devices". In addition, Parady shoes in Figure 3 that the register files have multiple registers, and each register reads and writes data from it. So, the registers must have a read and write port, making the registers each a two-ported random access memory device. Dreibelbis was relied upon to two effective read ports and one effective write port when there are multiple elements with multiple ports, i.e.

two or more ports, each. Dreibelbis explicitly states in column 6, lines 55-62 "...not all four sections may have banks simultaneously in operation, depending on the request activity from the processor. Anywhere from one to four banks may be simultaneously making transfers to/from port registers on the respective section..." Since one to four banks may transfer to/from, i.e. write/read, the port registers, depending on the request activity, it is possible for two banks to read data and one bank to write data simultaneously. Thereby, the limitations "two effective read ports and one effective write port" is met, since, according to those particular requests, there are two port registers reading data and one port register writing data.

35. The arguments seem to suggest that the random access memory devices have only two-ports each and that the "two effective read ports and one effective write port" is how the plurality of two-port only random access memory devices are accessed, e.g. the plurality of two-port only memory devices receive data by the same single effective write port and send data by the same two effective read ports, but this is not in the claim. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., plurality of two-ported random access memory devices and two effective read ports and one effective write port) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

36. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

37. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

38. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

39. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

40. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AJL
Aimee J. Li
4 March 2007

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100